

Amendments to the Claims

Kindly amend claims 1 & 14, and cancel claims 6-11, 13, 21-24 & 26 (without prejudice), as set forth below. All pending claims are reproduced below, with changes in the amended claims shown by strikethrough/double brackets (for deleted matter) and underlining (for added matter).

1. (Currently Amended) A method for providing arbitration for redundant controllers comprising:

providing logic for automatically determining which controller of redundant controllers is active controller, wherein outputs controlled by the redundant controllers are electrically connected together and provided as input to at least one device; [[and]]

providing an independent hardware interlock device coupled to the outputs of the redundant controllers to ensure that output controlled by only the active controller is enabled as input to the at least one device, the independent, hardware interlock device being separate from and external to the redundant controllers;

wherein providing the independent, hardware interlock device includes providing a hardware state machine to enable/disable outputs controlled by each controller of the redundant controllers and ensure that output of only the active controller is enabled as input to the at least one device;

further comprising employing a watch dog timer for each controller of the redundant controllers, and providing status of watch dog timer signals of the redundant controllers to the hardware state machine as input, wherein the hardware state machine employs the status of the watch dog timer signals of the redundant controllers to determine which controller of the redundant controllers to have output enabled for input to the at least one device; and

wherein providing the independent, hardware interlock device includes providing the hardware state machine for each controller of the redundant controllers, and wherein each hardware state machine further employs as input a unique identification of the associated controller.

2. (Original) The method of claim 1, further comprising providing a unique identification for each controller of the redundant controllers, wherein the automatically determining comprises employing the unique identifications to automatically determine which controller of the redundant controllers is active controller.
3. (Original) The method of claim 2, wherein the providing of unique identifications for the redundant controllers comprises providing hardwired identification bits for each controller of the redundant controllers.
4. (Original) The method of claim 1, further comprising providing logic for monitoring the active controller for possible failure, and upon detection of failure, for automatically switching active control to another controller of the redundant controllers.
5. (Original) The method of claim 4, wherein the monitoring comprises employing a watch dog timer for the active controller of the redundant controllers, and detecting failure of the active controller when the watch dog timer of the active controller expires.
6. (Canceled).
7. (Canceled).
8. (Canceled).
9. (Canceled).
10. (Canceled).
11. (Canceled).
12. (Canceled).
13. (Canceled).

14. (Currently Amended) A system for providing arbitration for redundant controllers comprising:

logic for automatically determining which controller of redundant controllers is active controller, wherein outputs of the redundant controllers are electrically connected together and provided as input to at least one device;
[[and]]

an independent, hardware interlock device coupled to the outputs of the redundant controllers to ensure that output controlled by only the active controller is enabled as input to the at least one device the independent, hardware interlock device being separate from and external to the redundant controllers; and

wherein the independent hardware interlock device includes a state machine for each controller of the redundant controllers, and wherein each state machine further employs as input a unique identification of the associated controller.

15. (Original) The system of claim 14, further comprising means for providing a unique identification for each controller of the redundant controllers, wherein the logic for automatically determining comprises means for employing the unique identifications to automatically determine which controller of the redundant controllers is active controller.

16. (Original) The system of claim 15, wherein the means for providing unique identifications for the redundant controllers comprises means for providing hardwired identification bits for each controller of the redundant controllers.

17. (Original) The system of claim 14, further comprising logic for monitoring the active controller for possible failure, and upon detection of failure, for automatically switching active control to another controller of the redundant controllers.

18. (Original) The system of claim 17, wherein the logic for monitoring comprises means for employing a watch dog timer for the active controller of the redundant controllers, and for detecting failure of the active controller when the watch dog timer of the active controller expires.

19. (Previously Presented) The system of claim 14, wherein the independent hardware interlock device includes a hardware state machine to enable/disable outputs controlled by each controller of the redundant controllers and ensure that output of only the active controller is enabled as input to the at least one device.

20. (Previously Presented) The system of claim 19, further comprising means for employing a watch dog timer for each controller of the redundant controllers, and for providing status of watch dog timer signals of the redundant controllers to the hardware state machine as input, wherein the hardware state machine employs the status of the watch dog timer signals of the redundant controllers to determine which controller of the redundant controllers to have output enabled for input to the at least one device.

21. (Canceled).

22. (Canceled).

23. (Canceled).

24. (Canceled).

25. (Canceled).

26. (Canceled).

27. (Canceled).

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